### MCA I Semester Supplementary Examinations July 2024 COMPUTER ORGANIZATION AND ARCHITECTURE

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		MCA I Semester Supplementary Examinations July 2024 COMPUTER ORGANIZATION AND ARCHITECTURE		
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Code	: 21	F00103	3,	
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		MCA I Semester Supplementary Examinations July 2024 COMPUTER ORGANIZATION AND ARCHITECTURE		
		(Master of Computer Applications)		
			: 60	
Time	e: 3 h	Answer all the questions  Explain about Machine Instruction Sequencing.  Discuss about basic input/output instructions.	,	
		Answer an the questions		
	/=\	Explain about Machine Instruction Sequencing.	6M	
1	(a) (b)	Discuss about basic input/output instructions.	6M	
¥	(5)	OR OR	6M	
2	(a)	Write about the 8086 Processor Addressing Modes	6M	
	(b)	Mention about Basic Computer Operational Concepts.		
3	(a)	Show the procedure for implementing fast multiplication.	6M 6M	
	(b)	Describe how to perform Multi-Programmed Control Logic.	OIVI	
		OR Discuss how to perform subtraction of two signed numbers.	6M	
4	(a) (b)	Explain in detail about the execution of a complete instruction.	6M	
	<b>(-</b> /		6M	
5	(a)	The state of the s	6M	
(*)	(b)	OR .		
6	(a)	What is Cache Memory? State its role in Memory System.	6M 6M	
1	(b)	What are the performance considerations followed while choosing the Secondary Storage Device?	OIVI	
7	(a)		6M 6M	
	(b)	What are the Interface circuits used in Data Transfer Activity? Explain working of any one approach.	OIVI	
		OR .		
8	(a)	Compare working of Standard I/O interfacing approach against DMA approach.	6M 6M	
	(b)	How to deal with Interrupt driven I/O access?	OIVI	
9	(a)	Elaborate about forms of Parallel processing.	6M	
	(b)	Write about Instruction Hazards.  OR	6M	
. 10	(a)	What is the need for Pipelining? Show its influence on Instruction sets.	6M	1
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6M

(b) Illustrate the structure of General purpose multiprocessors.

# MCA I Semester Regular & Supplementary Examinations February 2024

## COMPUTER ORGANIZATION AND ARCHITECTURE

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Cod	Code: 21F00103							
MCA I Semester Regular & Supplementary Examinations February 2024								
		COMPUTER ORGANIZATION AND ARCHITECTURE	20.0					
		(Master of Computer Applications)						
Tim	2.31	Max Max Max	arks: 60					
HIII	Time: 3 hours  Answer all the questions							
		Ariswer all the questions						
1	(a)	Answer all the questions  *****  Mention computer functional units and their operations.  Write about the 8086 processor data transfer instructions.  OR	6M					
1		Write about the 8086 processor data transfer instructions.	6M					
	(~)	OR						
2	(a)	Draw the general bus structure of the processor and explain its working.	6M					
	(b)	Discuss about basic input/output instructions.	6M					
			6M					
3	(a)	Discuss how to perform addition of two signed numbers.	6M					
	(b)	Explain in detail about the execution of a complete instruction.						
4	(a)	Show the procedure for implementing multiplication of positive numbers.	6M					
7	(b)	Describe how to perform hardwired control logic.	6M					
	(/							
5	(a)	What is cache memory? State is role in memory system.	6M					
	(b)	Present the concept of memory hierarchy using possible memory components.	6M					
		OR	6M					
6	(a)	What is virtual memory? Discuss about its applications.	6M					
	(b)	Describe the memory component selection process subjected to cost and speed.						
7	(a)	Explain working of Interrupt driven I/O.	6M					
	(b)	Illustrate working of DMA process.	6M					
		OR						
8	(a)	Explain how does the processor access its I/O devices.	6M					
	(b)	Compare working of Standard I/O interfacing approach against DMA approach.	6M					
1	4		6M					
9	(a)	State the need for Pipelining. Explain about its types.	6M					
(b) Draw and explain about Multiprocessors structures.  OR  6M								
10	(a)	What is role of data hazards? How to deal with it?	6M					
10	(a) (b)	Write about Interconnection Networks.	6M					
	(~)	This about more and						

#### courses a secure companies on acaptation than a committee of the companies COMPUTER ORGANIZATION & ARCHITECTURE

(For students admitted in 2021 & 2022 only)

Time: 3 hours

Max. Marks@6

#### Answer all the questions

t (a) With the help of a block schematic explain the basic organizational units of a discomputer.	
(b) Illustrate with an example explain different data instructions used in Assertin Language.  OR  2 (a) Compare and contrast multi processors and multi computer.  (b) Briefly explain Input output operations used in a computer.	61
2 (a) Compare and contrast multi processors and multi computer.	6N
	6M
3 (a) With the help of a flow chart explain how Booths multiplication algorithm works.	6M
(b) Explain the concept of Hardwired control unit.  OR	6M
4 (a) How integer division is performed in an ALU? Explain with suitable circuit.	6M
(b) With a neat diagram explain multi bus organization.	6M
5 (a) What is cache coherence and why (a) it important in shared memory multiprocessor systems? How can the problem to willed with a snoopy cache controller?	r 6M
(b) List out and explain performance considerations used in memory system.  OR	6M
6 (a) Explain any two memory and agement techniques.	6M
(b) Discuss about second storage devices.	6M
7 (a) Write a short nate on I/O and CPU Interface used in computer subsystem.	6M
(b) Discuss a content types of interrupts in I/O organization.  OR	6M
8 (a) Explain different types of buses used in Input output organization.	6M
(b) When the advantages and disadvantages of direct memory access.	6M
9 (a) Draw and explain SIMD array processor.	6M
(E) Explain data hazards with suitable example.  OR	6M
10 (a) Differentiate Instruction and Arithmetic Pipelines with an example.	6M
(b) What is instruction set? Explain briefly about some of instruction sets used in computer system.	6M

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