R21 Regulations JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR (Established by Govt. of A.P., ACT No.30 of 2008) ANANTHAPURAMU – 515 002 (A.P) INDIA

## MASTER OF COMPUTER APPLICATIONS

Course Code COMPUTER ORGANIZATION & ARCHITECTURE	L	Т	Р	С
21F <sup>0</sup> 0103	4	0	0	4
Semester	I		Ι	
Course Objectives:				
• Learn the fundamentals of computer organization and its relevance to classic	al a	nd		
modern problems of computer design				
• Understand the structure and behavior of various functional modules of a co	mpu	ter.		
• Discuss the contrigues that computers use to communicate with I/O devices	T			
• Study the concerts of pipelining and the way it can speed up processing.				
<ul> <li>Describe the basic characteristics of multiprocessors</li> </ul>				
<b>Course Outcomes (CO):</b> Sudent will be able to				
Demonstrate compute architecture concepts related to design of modern pro	cess	ors		
memories and I/Os		015,		
• Able to explore the hardwire equirements for cache memory and virtual me	emor	v		
Ability to design algorithms of valoit pipelining and multiprocessors	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	5		
• Ability to use memory and I/O services effectively				
<ul> <li>Detect nineline bazards and identify possible solutions to those bazards</li> </ul>				
UNIT I	Leo	oturo	Hree	
Basic Structure of Computer: Computer Type Functional Units Basic operation		ncer	te F	2110
Structure Software Performance Multiprocessors and Multicomputer		Jiecp	лз, г	Jus
Machine Instructions and Programs: Numbers, Autometic Operations and Programs	Inc	struct	ions	and
Instruction Sequencing Addressing Modes Basic Lup doutput Operations	, 1113	struct	10115	anu
INTEL-8086: CPU architecture Addressing modes - eneration of physical addre	SS - 1	code	segm	ent
registers. Zero, one, two, and three address instructions, INTEL 8086 ASSEMB	BLY	LAN	JGUA	AGE
INSTRUCTIONS-Data transfer instructions, input - output instructions, arithmetic.	log	tical s	shift,	and
rotate instructions, Conditional and unconditional transfer.		,	,	
UNIT – II	Leo	cture	Hrs:	
Arithmetic: Addition and Subtraction of Signed Numbers, Design of Fast Adders	, Mu	ltipli	catio	n of
Positive Numbers, Signed-operand Multiplication, Fast Multiplication Integer Divis	sion,	Floa	ting-	Point
Numbers and Operations.				
Basic Processing Unit: Fundamental Concepts, Execution of a Complete Instruc	tion,	, Mul	tiple-	Bus
Organization, Hardwired Control, Multi-programmed Control.				
UNIT - III	Leo	cture	Hrs:	
The Memory System: Basic Concepts, Semiconductor RAM Memories, Read-Only	Mer	norie	s, Sp	eed,
Size and Cost, Cache Memories, Performance Considerations, Virtual Memorie	emo	ry Ma	anage	ement
Requirements, Secondary Storage.				
UNIT – IV	Lec	ture	Hrs:	
Input/output Organization: Accessing I/O Devices, Interrupts, Processor Examples, I	Dire	et Me	emory	/
Access, Buses, Interface Circuits, Standard I/O Interfaces.		S		
UNIT – V				
Pipelining: Basic Concepts, Data Hazards, Instruction Hazards, Influence on Instruct	tion	Sets.	$\sim$	
Large Computer Systems: Forms of Parallel Processing, Array Processors, The Stru	ıctur	e of	Gene	eral-
Purpose multiprocessors, Interconnection Networks.			•	
TEXT BOOKS:				
1 Computer Organization Carl Hamacher ZuonkoVranesia SoftwatZaky MaCrow	ц;11	E,	lucat	ion
5th Edition 2013	11111	Ľ	uuual	1011,
2. Microprocessors and Interfacing. Douglas Hall, Tata McGraw-Hill.				